PLEASE AMEND THE ABSTRACT

Please replace the original Abstract with the amended Abstract below.

ABSTRACT

An improved borderless contact structure for salicide field effect transistors (FETs) has been achieved. Salicide FETs are formed on device areas surrounded by a shallow trench isolation (STI) using a first rapid thermal anneal to form a metal silicide on the source/drain contacts and the gate electrodes. An interlevel dielectric (ILD) layer is deposited, and borderless contact openings, extending over the STI, are etched in the ILD to the source/drain areas. When the contact openings are etched, this results in over-etched regions in the STI at the source/drain-STI interface that result in source/drain-to-substrate shorts when metal plugs are formed in the contact openings. A contact opening implant is used to dope the junction profile in the source/drain contact around the STI over-etched region to prevent electrical shorts. The second RTA is used to concurrently reduce the silicide sheet resistance and to electrically activate the contact opening implanted dopant.